

WHAT IS CLAIMED IS:

1 1. A method of processing data packets comprising:
2 generating an enqueue command specifying a queue
3 descriptor associated with a new buffer in response to
4 receiving an enqueue request, with the queue descriptor stored
5 in a cache and the queue descriptor having a head pointer
6 pointing to a first buffer in a queue of buffers and a tail
7 pointer pointing to a last buffer in the queue of buffers and
8 with the first buffer having a buffer pointer pointing to a
9 next buffer in the queue;

10 setting a buffer pointer associated with the last buffer
11 to point to the new buffer; and

12 setting the tail pointer to point to the new buffer.

1 2. The method of claim 1 further comprising:

2 setting the tail pointer to point to another buffer in
3 response to receiving an enqueue request with respect to said
4 other buffer.

1 3. The method of claim 1 further comprising:

2 generating a dequeue command specifying the queue
3 descriptor associated with the first buffer in response to
4 receiving a dequeue request with respect to the first buffer,
5 and setting the head pointer to point to the next buffer.

1 4. The method of claim 3 further comprising:

2 setting the head pointer to point to a buffer pointed to
3 by the next buffer in response to receiving a dequeue request
4 with respect to the next buffer.

1 5. The method of claim 1 comprising:

2 replacing a queue descriptor with the queue descriptor
3 associated with the new buffer, if the queue descriptor
4 associated with the new buffer is not in the cache.

1 6. An apparatus for processing data packets comprising:

2 a first memory comprising:

3 a queue of buffers, having a first buffer with a
4 buffer pointer pointing to a next buffer in the queue,
5 and

6 a cache of queue descriptors, each of which has a
7 head pointer pointing to the first buffer in the queue,
8 and a tail pointer pointing to a last buffer in the
9 queue;

10 a processor coupled to the first memory; and

11 a computer-readable medium storing instructions that when
12 applied to the processor, cause the processor to:

13 generate an enqueue command specifying a queue
14 descriptor associated with a new buffer, in response to

15 receiving an enqueue request associated with the new
16 buffer,

17 set a buffer pointer associated with the last buffer
18 to point to the new buffer, and

19 set the tail pointer to point to the new buffer.

1 7. The apparatus of claim 6 wherein the processor is
2 configured to:

3 set the tail pointer to point to the other buffer, in
4 response to receiving an enqueue request with respect to
5 another buffer.

1 8. The apparatus of claim 6 wherein the processor is further
2 configured to:

3 generate a dequeue command specifying a queue descriptor
4 associated with the first buffer and set the head pointer to
5 point the next buffer in response to receiving a dequeue
6 request with respect to the first buffer.

1 9. The apparatus of claim 8 wherein the processor is
2 configured to:

3 set the head pointer to point to a buffer pointed to by
4 the next buffer in response to receiving a dequeue request
5 with respect to the next buffer.

1 10. The apparatus of claim 6 wherein the processor is
2 configured to:

3 replace a queue descriptor with the queue descriptor
4 associated with the new buffer, if the queue descriptor
5 associated with the new buffer is not in the cache.

1 11. The apparatus of claim 10 wherein the processor is
2 further configured to replace a queue descriptor based on a
3 least recently used (LRU) policy.

1 12. The apparatus of claim 6 wherein each buffer in the queue
2 includes pointers to data buffers having data packets residing
3 in a second memory.

1 13. The apparatus of claim 6 wherein the cache of queue
2 descriptors includes approximately 16 queue descriptors.

1 14. The apparatus of claim 6 wherein each buffer in the queue
2 includes a count field having a value representing the number
3 of buffers in the queue.

1 15. The apparatus of claim 6 wherein the queue is a linked
2 list of buffers.

1 16. An article comprising a computer-readable medium that
2 stores computer executable instructions for causing a computer
3 system to:

4 generate an enqueue command specifying a queue descriptor
5 associated with the new buffer in response to receiving an
6 enqueue request, the queue descriptor being stored in a cache
7 of queue descriptors, the queue descriptors having a head
8 pointer pointing to a first buffer in a queue and a tail
9 pointer pointing to a last buffer in the queue, the first
10 buffer having a buffer pointer pointing to a next buffer in
11 the queue;

12 set a buffer pointer associated with the last buffer to
13 point to the new buffer; and

14 set the tail pointer to point to the new buffer.

1 17. The article of claim 16, including instructions for
2 causing the computer to:

3 set the tail pointer to point to the other buffer in
4 response to receiving an enqueue request with respect to
5 another buffer.

1 18. The article of claim 16, including instructions for
2 causing the computer to:

3 generate a dequeue command specifying the queue
4 descriptor associated with the first buffer and set the head
5 pointer to point to the next buffer, in response to receiving
6 a dequeue request with respect to the first buffer.

1 19. The article of claim 18, including instructions for
2 causing the computer to:

3 set the head pointer to point to a buffer pointed to by
4 the next buffer, in response to receiving a dequeue request
5 with respect to the next buffer.

1 20. The article of claim 16, including instructions for
2 causing the computer to:

3 replace a queue descriptor with the queue descriptor
4 associated with the new buffer, if the queue descriptor
5 associated with the new buffer is not in the cache.

1 21. A system comprising:

2 a source of data packets grouped into data buffers;

3 a destination for the data buffers; and

4 an apparatus coupled to the source of the data packets
5 and to the destination of the data buffers, the apparatus
6 comprising:

7 a first memory comprising:

8 a queue of buffers having a first buffer
9 with a buffer pointer pointing to a next buffer in
10 the queue, and

11 a cache of queue descriptors, each of which has
12 a head pointer pointing to the first buffer in the

13 queue and a tail pointer pointing to a last buffer
14 in the queue, and

15 a processor coupled to the first memory, and
16 a computer-readable medium storing instructions that
17 when applied to the processor, cause the processor to:

18 generate an enqueue command specifying a queue
19 descriptor associated with a new buffer,

20 set a buffer pointer associated with the last
21 buffer to point to the new buffer, and

22 set the tail pointer to point to the new
23 buffer.

1 22. The system of claim 21 wherein the processor is further
2 configured to:

3 set the tail pointer to point to the other buffer, in
4 response to receiving an enqueue request with respect to
5 another buffer.

1 23. The system of claim 21 wherein the processor is further
2 configured to:

3 generate a dequeue command specifying a queue descriptor
4 associated with the first buffer and set the head pointer to
5 point to the next buffer, in response to receiving a dequeue
6 request with respect to the first buffer.

1 24. The system of claim 23 wherein the processor configured
2 to:

3 set the head pointer to point to a buffer pointed to by
4 the new buffer, in response to receiving a dequeue request
5 with respect to the new buffer.

1 25. The system of claim 21 wherein the processor is
2 configured to:

3 replace a queue descriptor with the queue descriptor
4 associated with the next buffer, if the queue descriptor
5 associated with the next buffer is not in the cache.

1 26. The system of claim 21 wherein the processor is further
2 configured to replace a queue descriptor based on a least
3 recently used (LRU) policy.

1 27. The system of claim 21 wherein each buffer in the queue
2 includes pointers to data buffers containing data packets
3 residing in a second memory.

1 28. The system of claim 21 wherein the cache of queue
2 descriptors includes approximately 16 queue descriptors.

1 29. The system of claim 21 wherein each buffer in the queue
2 includes a count field having a value representing the number
3 of buffers in the queue.

1 30. The system of claim 21 wherein the queue is a linked list
2 of buffers.